REMARKS

Claims 1-18 are pending in the application and stand rejected.

Rejection under 35 U.S.C §102

Claims 1-15, 17 and 18 stand rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,708,830 to Stein. In particular, the Examiner finds that, with regard to claim 1, Stein discloses all of the claimed limitations. . .

The Examiner asserts that the claimed decoupling element is anticipated by Stein's "elements 6, 18 and 14." Applicants submit that this is an overly broad reading of the claim limitation in view of the plain language of the reference. Element 6 is "a writable control store 6 mapped into the memory area of the host" that the address bus communicates with (col. 2 ll. 54-56). "So far as internal operation of the coprocessor is concerned, the writable control store 6 operates only in read mode, addressable as 2K of 56 bit words, the seven blocks being enabled simultaneously for reading a word, identified by an eleven bit address from a sequencer 14, into a 56 bit wide pipeline latch 16. Sixteen bits of the output from the pipeline communicate with the bus DBUS, the remaining 40 bits of the output forming control signals for various components of the coprocessor as described further below." (col. 3 ll. 3-11)

Element 18 is a microprocessor that is also referred to as the intermediate processor, and which communicates with an intermediate bus DBUS that also connects with, among others, element 14. Element 14 is a sequencer which, in run mode, "issues addresses to the writable control store 6 under control of a clock signal, typically at 5 MHz, the address sequence being in accordance with a control signal received by the microprocessor. The 56 bit word selected from the control store 6 by an address from the microsequencer is latched by the pipeline latch 16 for one clock cycle. This word comprises control signals and instructions for the GAPP array 3 and its associated buffers and rotators and/or for the microprocessor 18 and/or for the microsequencer 14, as detailed above, which are acted on accordingly." (col. 5 ll. 48-58)

What is important to understand is that the system of Stein has two different modes of operation: a boot mode and a run mode. Instructions are loaded into the writable control store 6

only during the boot mode (col. 2 ll. 58-63), during which the sequencer is disabled (col. 5 ll. 31-32). During the run mode, when the host processor and the coprocessor run asynchronously, only data to be operated on is transferred to the coprocessor (col. 2 l. 63 – col. 3 l. 2), and this is the only mode during which the sequencer is enabled (col. 5 ll. 36-45).

Claim 1, on the other hand, recites that computations are passed to the second processor from the first processor through the decoupling element such that the second processor executes computations passed from the first processor through the decoupling element. This is clearly not possible in the system of Stein because at least part of what the Examiner likens to the claimed decoupling element is disabled while instructions are being passed to the coprocessor (during the boot mode).

Applicants further note that the Examiner views the sequencer 14 not only as a subpart of the alleged decoupling element of Stein, but also assigns it double duty as the claimed coprocessor controller. This reading is clearly at odds with itself. The sequencer 14 is either a coprocessor controller that controls the activity of the second processor to ensure execution of the second processor is correctly ordered with respect to loads from memory, or it is a decoupling element through which computations are passed to the second processor from the first processor such that the second processor executes computations passed from the first processor through the decoupling element and this execution of computations by the second processor is decoupled from the operation of the first processor - it cannot be both.

Applicants submit that Stein is fundamentally different from the claimed invention because it operates in a fundamentally different manner. Stein switches between two different modes, boot and run, to either load instructions or to execute these instructions, respectively. The system of claim 1 clearly does not require such different modes of operation because of the presence of the decoupling element, which allows the first processor to pass computations to the second processor while the second processor is executing other computations. There is no such decoupled operation taking place in Stein.

To make the above-discussed differences between the prior art and the presently claimed invention clearer and thereby ease the passage of the present application to allowance, Applicants have further amended claim 1 to specifically recite that the second processor executes

computations passed from the first processor through the decoupling element while the first processor is providing further instructions to the decoupling element.

In view of the above, Applicants respectfully submit that Stein does not in fact anticipate amended claim 1, and request the Examiner to kindly reconsider and pass this claim to issue.

Claims 2-15 and 17 depend from claim 1. In view of the above discussion, it is submitted that claim 1 is allowable, and for this reason claims 2-15 and 17 are also allowable.

Claim 18 is a method claim that corresponds to apparatus claim 1 and that includes the step of passing instructions to a second processor for executing a task. As elaborated upon above, this is a different method of operating than that disclosed by Porter, wherein only data (not instructions) is passed to the vector processor for processing thereof. Applicants note with particularity that claim 18 recites identifying part of a code as providing a task to be carried out by the second processor, and then passing information defining the task to a decoupling element, which then passes instructions derived from this information. A careful read of the passages cited by the Examiner in Stein reveals that this is simply not disclosed by Stein and, should the Examiner insist, Applicants respectfully request her to specifically note the precise column and line where each of these limitations is taught, as per the requirements set forth in 37 C.F.R. 1.104(c)2. Furthermore, as elaborated upon previously, Stein loads all instructions to be carried out by the coprocessor during the boot mode, and also does not in fact have a decoupling element.

In addition, and in the spirit of cooperation, Applicants have amended claim 18 in a manner similar to claim 1, to specifically recite that the second processor executes the instructions passed from the decoupling element while the first processor passes further information defining the task to the decoupling element. Thus, Applicants respectfully submit that this claim, as presently amended, is also novel and allowable over Porter.

Rejection under 35 U.S.C §103

Claims 16 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Stein in view of the Hennessy article. Claim 16 depends from claim 1. "If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious." *In re*

Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). Therefore, in light of the above discussion of claim 1, Applicants submit that claim 16 is also allowable.

In view of the above, Applicants submit that the application is now in condition for allowance and respectfully urge the Examiner to pass this case to issue.

The Commissioner is authorized to charge any additional fees which may be required or credit overpayment to deposit account no. 08-2025. In particular, if this response is not timely filed, the Commissioner is authorized to treat this response as including a petition to extend the time period pursuant to 37 CFR 1.136(a) requesting an extension of time of the number of months necessary to make this response timely filed and the petition fee due in connection therewith may be charged to deposit account no. 08-2025.

I hereby certify that this correspondence is being deposited with the United States Post Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on

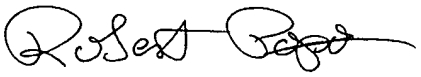
October 24, 2005
(Date of Transmission)

Mia Kim
(Name of Person Transmitting)

(Signature)

10/24/05
(Date)

Respectfully submitted,



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